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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H04J 3/02

A1

(11) International Publication Number: **WO 96/19053**

(43) International Publication Date: 20 June 1996 (20.06.96)

(21) International Application Number: PCT/US95/16470

(22) International Filing Date: 15 December 1995 (15.12.95)

(30) Priority Data:
08/356,999 16 December 1994 (16.12.94) US

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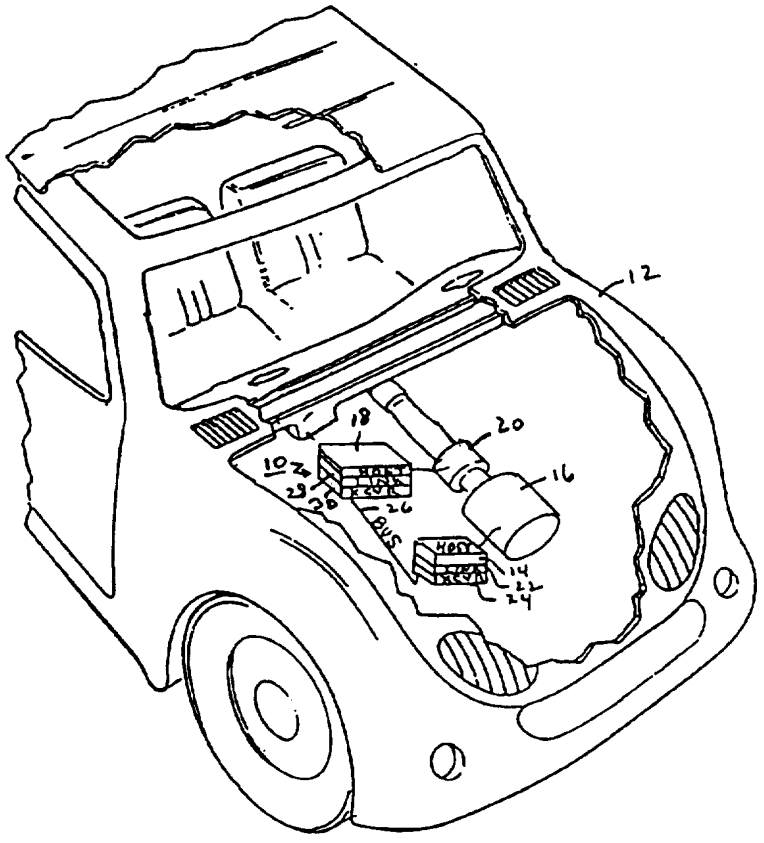
(81) Designated States: AM, AT, AU, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LT, LU, LV, MD, MG, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TT, UA, UG, US, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, LS, MW, SD, SZ, UG).

Published
With international search report.

(54) Title: VEHICLE COMMUNICATIONS BUS LINK WITH STATE MACHINE

(57) Abstract

A state machine communications link (22) for a vehicle (12) interconnects a host microprocessor (14) that is associated with a vehicle component (e.g., the engine (16), to a communications bus (26). Other host microprocessors (18) of the vehicle (12) are likewise connected to the bus (26), such that the various hosts (14, 18) communicate. The state machine link (22) undertakes certain communications tasks on behalf of the host (14) with which it is associated. For example, the state machine link (22) appends start of frame (SOF) symbols (34) to host messages (32) prior to transmission of the messages over the bus (26). Also, the link (22) appends end of frame (EOF) and end of data (EOD) symbols (46, 40) to messages, as well as check byte (CRC) symbols (38). Most, but not all, data transfer between the host (14) and link (22) is unsolicited by the host (14).



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VEHICLE COMMUNICATIONS BUS LINK WITH STATE MACHINE

FIELD OF THE INVENTION

The present invention relates generally to vehicle communication networks, and more particularly to vehicle communication bus links.

BACKGROUND

Many modern vehicles incorporate microprocessors to control the operations of various components. As but two examples, the operation of an engine can be controlled by an engine microprocessor, often colloquially referred to as a "host", while the operation of a transmission can be controlled by a transmission microprocessor, also referred to as a "host".

It is frequently the case that one host microprocessor of a vehicle must communicate with one or more other host microprocessors. For example, the transmission host might require data pertaining to engine speed, and this data might be resident in the engine host. Accordingly, the various host microprocessors of a vehicle are often electrically connected to a communications bus, to facilitate the sharing of data between hosts. The current U.S. industry standard communications bus is referred to as a J1850 bus.

It will be appreciated that data communication over a bus requires that data messages be formatted, encoded, transmitted, received, decoded, checked for errors, possibly acknowledged, as well as various other communications protocol activities. It will be further appreciated that the computational time spent by a host in undertaking such communication activities reduces the time available for the host to undertake its principal function, namely, the control and monitoring of the associated vehicle component. Still further, design flexibility can be undesirably reduced when a single component, i.e., a host, must be programmed to execute more than a single task, e.g., engine control.

As recognized herein, however, it is cost effective to provide a hardware-based communications interface link which can undertake some or all of the data communications tasks on behalf of a host microprocessor in a vehicle. As further recognized by the present invention, such a hardware link, in addition to being cost-effective, can also perform certain communications functions faster than a software-implemented link.

Accordingly, it is an object of the present invention to provide a communications interface link for linking a host microprocessor to a communications bus in a vehicle. Another object of the present invention is to provide a communications interface link that can undertake selected communications

activities in transmitting data messages between a host microprocessor and a vehicle's communications bus. Still another object of the present invention is to provide a communications interface link that is easy to use and cost-effective.

SUMMARY OF THE INVENTION

A communications link for transmitting data between a host microprocessor (host) in a vehicle and a communications bus includes a signal encoder/decoder (SED). The SED is electrically connected, preferably via a bus transceiver, to the bus for converting bus signals from the bus to corresponding link signals and for converting link signals to corresponding bus signals. A byte buffer is electrically connected to the host for solicited reception of a first byte of data of a first message from the host when the host generates a byte ready signal, and for unsolicited serial reception of subsequent bytes of the first message thereafter. Additionally, the link includes a state machine which is electrically connected to the byte buffer and SED.

In accordance with the present invention, the state machine embodies logic for establishing data transmission through the link. More specifically, the state machine causes the SED to transmit to the bus a data message including the bytes of the first message. Further, the state machine causes the generation of a start of frame (SOF) symbol only when either: the communications bus is idle, or a predetermined voltage occurs on the communications bus within a predetermined period. Also, the state machine preferably causes a byte received from the SED to be transmitted to the host without solicitation from the host.

In the presently preferred embodiment, the state machine further causes the appending of end of data (EOD) symbols and end of frame (EOF) symbols to the data message. Preferably, the link includes a status/control circuit (RSSTATE) which is electrically connected to the state machine and host for transmitting status bytes to the host in response to a status signal therefrom and for receiving control bytes from the host.

As intended by the preferred embodiment, the state machine appends an in-frame response to the data message in response to a predetermined control message received from the host by the RSSTATE. Also, the state machine preferably includes a bit counter for counting bits during data transmission and reception. Per the presently preferred embodiment of the invention, the state machine causes an SOF symbol to be transmitted in response to a byte ready signal from the host.

Using the preferred logic, the state machine causes a byte after the first byte of the first message to be received unsolicited into the byte buffer after the immediately preceding byte has been transmitted. Moreover, in the preferred link the state machine appends a CRC symbol to the data message when no CRC symbol has previously been appended to the message.

In another aspect of the present invention, a vehicle is disclosed which includes a communications bus. A plurality of component host microprocessors (hosts) are provided, with each

host being electrically connected to the communications bus via a respective link. Each link is characterized by logic circuitry for performing method steps to transmit and receive messages between the hosts via the communications bus. In accordance with the present invention, each link includes a state machine embodying logic for establishing data transmission through the link, the state machine causing the link to transmit to the bus a data message including the bytes of a first message, the state machine further causing the generation of a start of frame (SOF) symbol only when either: the communications bus is idle, or a predetermined voltage occurs on the communications bus within a predetermined period.

In still another aspect of the present invention, a state machine link is disclosed for interconnecting a host microprocessor (host) in a vehicle to a communications bus in the vehicle. The link includes buffer means for receiving a first byte of a first message from the host in response to a solicitation signal from the host. Moreover, the link includes means for causing bytes of the first message subsequent to the first byte to be serially received into the buffer means. Also, the link includes means for transmitting a start of frame (SOF) symbol onto the bus in response to the solicitation signal only when: the bus is idle, or a voltage transition is present on the bus.

The details of the present invention, both as to its structure and operation, can best be understood in reference to the accompanying drawings, in which like reference numerals refer to like parts, and in which:

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a perspective view of a vehicle incorporating a plurality of host microprocessors and a communications link, with portions shown schematically;

Figure 2 is a schematic diagram of a communications message;

Figure 3 is an electrical schematic diagram of the vehicle communications bus link with state machine of the present invention, in four sub-figures (3A-3D); and

Figure 4 is a state diagram showing the logic of the present invention, in four sub-figures (.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring initially to Figure 1, a vehicle communication system is shown and generally designated 10, for linking microprocessors in a vehicle 12. As shown, the system 10 includes at least a first host microprocessor (host) 14 that is electrically connected to controls in the engine 16 of the vehicle 12, for controlling operation of the engine 16. Further, the system 10 includes at least a second host microprocessor (host) 18 that is electrically connected to controls in the transmission 20 of the vehicle 12, for controlling operation of the transmission 20. Additional hosts (not shown) can

be included in the system 10. In one presently preferred embodiment, each host 14, 18 is a type M68HC05 microprocessor.

Figure 1 shows that the first host 14 is electrically connected to a respective state machine-based hardware communications link 22. In turn, the link 22 is electrically connected to a respective bus transceiver 24 which, among other things, converts digital signals from the link 22 to analog signals for output onto a communications bus 26. In one presently preferred embodiment, the bus transceiver 24 is a HIP-7020 chip made by Harris Corp. of Melbourne, Florida, and the communications bus 26 is a single wire J1850 bus conforming to J1850 bus standard protocol as established by the Society of Automotive Engineers (SAE).

Likewise, the second host 18 is electrically connected to a respective state machine-based hardware communications link 28 that is in all essential respects identical in configuration and operation to the link 22. In turn, the link 28 is electrically connected to a respective bus transceiver 30, with the transceiver 30 being connected to the communications bus 26. For simplicity of disclosure, the discussion below focusses on the link 22. It is to be understood, however, that the discussion below pertains equally to all of the links in the system 10.

Figure 2 shows a typical message conforming, in the presently preferred embodiment, to J1850 bus protocol that might be generated by one of the hosts 14, 18 and transmitted over the bus 26. As shown, the message is characterized by a message frame 32 which includes a start of frame (SOF) symbol 34 and one or more data bytes 36. The message frame 32 also includes a check byte (CRC) 38, used for error detection purposes. Together, the SOF symbol 34, data bytes(s) 36, and CRC 38 establish the main body of the message frame 32.

Additionally, the message frame 32 includes an end of data symbol 40 and, in some instances, a normalization bit 42 which is immediately followed by an in frame response (IFR) byte or bytes 44. An end of frame (EOF) symbol 46 follows the IFR byte 44. After a predetermined time period, the EOF symbol 46 (and message frame 32) terminates at reference numeral 48, after which period the bus 26 is considered to be idle. Together, the normalization bit 42, IFR byte(s) 44, and EOF symbol 46 establish an in frame response of the message frame 32. The SOF symbol 50 of another succeeding message might then appear on the bus 26.

As more fully disclosed below, the purpose of the present invention is to provide a cost-effective, fast link for preparing the message frame 32 based upon data bytes 36 received from a host microprocessor, without requiring host operation for each communications step, e.g., appending SOF, EOD, and EOF symbols, as well as CRC bytes, to the data bytes 36. It is to be understood that this purpose is fulfilled in the communications link 22 of the present invention by logic undertaken by a state machine within the link 22. In accordance with principles known in the art, the logic of the state machine of the link 22 is established by a plurality of flip-flops, the output signals of which establish

the particular current state of the state machine, in combination with a plurality of logic gates which establish the next subsequent state of the state machine based upon the state machine inputs from the various other components of the link 22.

Now referring to Figure 3, the details of the link 22 can be seen. As shown, the link 22 includes a state machine that is established by a main state (MSSTATE) circuit 52, a state machine input (STATIN) circuit 54, and a state machine output (STATEOUT) circuit 56. Additionally, the link 22 includes a signal encoder-decoder (SED) circuit 58 which is connected to the bus transceiver 24 (Figure 1) via output pin "transmit" and input pin "receive". The function of the SED 58 is to encode data messages as appropriate for subsequent transmission onto the bus 26, and to decode data from the bus 26 for use by the link 22. The SED 58 also facilitates proper timing of message bits for transmission/reception.

Moreover, the link 22 includes a request status (RSSTATE) state machine 60 which responds to status requests from the host 14. Further, the link 22 includes a vector circuit 62. The vector circuit 62 resets the state machine of the present invention upon the occurrence of various errors and bus breaks.

An 8-bit byte buffer 64 is included in the link 22, for transferring data therethrough between the link 22 and host 14. Also, a check byte (CRC) generator circuit (CRCGEN) 66 is provided for generating CRC bytes to be appended to outgoing messages, while a CRC check circuit (CRCCHECK) 68 checks CRC bytes in incoming messages for error detection. An encoder circuit 70 can be configured to drive the SED 58 to transmit bits in the byte buffer 64 onto the bus 26, in response to signals from the STATEOUT circuit 56.

Figure 3 shows the various electrical interconnections between the components discussed above. Of note are input connections from the host 14, symbolized in Figure 3 by hollow arrows having respective lines connected to the arrow tips. These input connections are denoted in Figure 3 as "REQSTAT" (shown as an input to the RSSTATE 60 and used for communicating status requests from the host 14 to the link 22) and master in-slave out ("MISO") (shown as an input to the CRCGEN 66, RSSTATE 60, and STATEIN 54, for communicating message data bits to the link 22). Also, an input denoted "RESETL", shown as input to most of the circuit components of the link 22, transmits reset signals from the host 14 to the link 22, although a separate reset circuit may be provided to reset both the host 14 and link 22. Furthermore, an input from the host 14 is provided to the STATEIN 54 via input pin "BYTE" to indicate that the data buffer of the host 14 contains data to be transferred to the link 22.

Additionally, output connections are provided to communicate data to the host 14 from the link 22. As shown, the output connections are symbolized in Figure 3 by hollow arrows having respective lines connected to the bases of the arrows. The output connections include an IDLEPIN

for communicating to the host 14 that an idle condition exists on the bus 26. Also, an output connection master out-slave in ("MOSI") is used to send message data bits to the host 14, while SACTIVL and SPISCK pins communicate timing signals to the host 14.

The input and output connections transmit data between the host 14 and link 22 via a two-way serial peripheral interface (SPI) bus. With the logic described below, the link 22 is the bus master, providing the synchronous clock signal. When the link 22 desires to use the SPI bus, the SACTIVE pin pulls a slave select pin of the host 14 low. The host 14, however, is the SPI bus master when the link 22 is not using the bus.

High level NOR, OR, and AND gates, generally designated 72, interconnect the byte buffer circuit 64 and CRC generator 66. Additional high level OR and AND gates, generally designated 74, interconnect various link 22 components with certain output connections to the host 14, i.e., the MOSI (data output) and serial peripheral connection clock (SPISCK) connections. Lower level logic components within the various circuits are configured by means well-known in the art to effect the logic disclosed below in reference to Figure 4. Link output and input busses, respectively labelled SO(29:0) and SI(33:0) in Figure 3, establish main communication busses within the link 22. The signal on the output bus SO(29:0) represents the current state of the main state machine (MSSTATE) 52. Consequently, the signal on the SO(29:0) bus functions to configure the components of the link 22 as appropriate for the current state of the link 22, as defined by the logic circuits within the MSSTATE 52.

Various other communications lines are shown and conventionally labelled in Figure 3. Some of these lines carry routine data (e.g., clocking/timing signals) that are within the purview of the skilled artisan and will not be discussed further. Other of these lines carry particular data of the present invention and will be discussed further below in connection with the description of the logic of the link 22.

Now referring to Figure 4, the logic of the link 22 can be appreciated. States of the state machine of the present invention are shown as rectangles and denoted as ST [#], wherein the pound sign represents an integer representative of a particular state. On the other hand, inputs to the state machine are shown as decision diamonds. When the disclosure below speaks of the state machine "determining" whether particular events have occurred, it is to be understood that what is being determined is whether particular inputs representative of the events have been received by the link 22.

After initial power-up or reset, the link 22 is in state 0 (ST 0), and immediately moves to state 1 (ST 1). In the first state, a signal "XMITMODE" is cleared. More particularly, in ST 1 the encoder 70 is not enabled to drive the SED 58 to transmit data onto the bus 26.

From ST 1, the link 22 might receive an input, at decision diamond 80, through the SED 58 that indicates that an end of frame (EOF) signal is present on the bus 26. If it is, the state machine

moves to state 2 (ST 2). The "no" loop shown in Figure 4 simply indicates that the state machine remains in ST 1 until an EOF symbol is detected on the bus 26.

At ST 2, "XMITMODE", "byte ready", and "last byte" flags are cleared and the "CRC OK" circuit of ST 23, discussed more fully below, is enabled. The "byte ready" and "last byte" flags, when set, respectively indicate to the link 22 that the host 14 has signalled that it contains a byte to be transmitted, and that the byte is the last byte of the host's message.

From ST 2, the MSSTATE 52 determines, at diamond 82, whether the bus 26 is idle based upon the signal from the SED 58 as transmitted through the STATEIN 54, and if so proceeds to ST 3. Otherwise, the MSSTATE 52 proceeds to diamond 84 to determine whether a voltage transition is present on the bus 26. If not, the link 22 returns to ST 2. In contrast, if the test at either diamond 82 or 84 is positive, the link 22 is configured for ST 3.

In ST 3, the MSSTATE 52 causes the link 22 to clear the following flags, which have the representations indicated:

end of data (EOD) - when set, indicates that an EOD signal has been received by the SED 58 from the bus 26;

Acker - when set, indicates that the host 14, via the REQSTAT input to the RSSTATE 60, has signalled that the host 14 desires to send an acknowledgement to a message received by the host 14;

Macker - when set, indicates that the host 14, via the REQSTAT input to the RSSTATE 60, has signalled that the particular acknowledgement desired to be appended is a so-called (per J1850 protocol) "type 3" acknowledgement.

Send CRC - set by the MSSTATE 52 to indicate that the link 22 has appended a check byte or bytes (CRC) to a message being processed;

OK to ack - used in conjunction with the "Acker" flag. Because the "Acker" flag might be set by the host 14 immediately after the first byte of a multi-byte message is received, and the subsequent bytes of the message could be corrupted, it is necessary to include the "OK to ack" feature to ensure an acknowledgement of a corrupted message is not sent. When set, the "OK to ack" flag indicates that the host 14 has signalled it has a byte ready for transmission during a CRC byte transfer, thereby ensuring the entire received message that is to be acknowledged has been received satisfactorily prior to transmitting an acknowledgement of the message.

Additionally, at ST 3 a bit counter, which counts the number of bits in the byte buffer 64, is reset, and the idle pin output of the STATOUT 56 to the host 14 is set to indicate an idle condition on the bus 26.

Next, the MSSTATE 52 again determines, at diamond 86, whether the bus 26 is idle. If it is, the MSSTATE 52 determines, at diamond 88, whether the host 14 has asserted (via the byte input pin to the STATEIN 54) that the communication buffer of the host 14 contains a byte to be transmitted onto the bus 26. If a byte is ready to be transmitted by the host 14, the MSSTATE 52 determines at diamond 90 whether the host 14 has requested a status byte exchange from the link 22. Such a request is made by the host 14 via input pin REQSTAT to the RSSTATE 60. If no such request has been made, the MSSTATE 52 proceeds to ST 5. If no byte is ready at diamond 88, the MSSTATE remains in ST 3 as shown by the "no" loop from diamond 88.

If, on the other hand, the MSSTATE 52 determines, at diamond 86, that the bus 26 is no longer idle, the MSSTATE proceeds to ST 4, wherein the idle pin is reset to so indicate the condition of the bus 26. The MSSTATE 52 next determines, at diamond 92, whether a byte is ready to be transmitted from the host 14. If not, the MSSTATE 52 determines at diamond 94 whether a high to low voltage transition, indicating the detection by the SED 58 of the falling edge of a start of frame (SOF) symbol previously transmitted onto the bus 26 by a link other than the link 22, is present on the bus 26. If it is, the MSSTATE proceeds to ST 9, wherein the CRC circuits 66, 68 are reset prior to proceeding to ST 10. If, on the other hand, a transition is not present, the link 22 remains in ST 4.

If, at diamond 92, the MSSTATE 52 determined that a byte was ready for transmission from the host 14, then the MSSTATE 52 determines at diamond 96 whether the bus 26 non-idle condition was caused by the transmission of an SOF signal from a link other than the link 22, within a predetermined time period (currently 128μS). If so, the MSSTATE 52 proceeds to ST 5, but if not, the MSSTATE 52 proceeds to ST 25 to set an error detection status bit. This bit will be transmitted over the SPI bus from the RSSTATE 60 to the host 14 when the host 14 transmits a REQSTAT bit to the link 22. The link 22 then resets to ST 0. This last step is effected in the presently preferred embodiment by generating a signal on the VECRSTL line from the vector 62. Thus, the link 22 is reset if a SOF symbol is detected on the bus 26 and the link 22 is not in ST 4 (or, as more fully disclosed below, in ST 8).

As disclosed more fully below, at ST 5 the link 22 transmits an SOF symbol onto the bus 26. Thus, it can be appreciated at this point that the link 22 transmits an SOF symbol only when either: the communications bus 26 is idle, or a predetermined voltage occurs on the communications bus 26 within a predetermined period, indicating that another link has recently transmitted an SOF and consequently that the link 22 can concurrently transmit a message onto the bus 26.

Recall that at diamond 90, the MSSTATE 52 determined whether the host 14 had requested a status report via a status byte transfer. When the host 14 requests a status byte transfer, the link 22 latches a flag indicating that "REQSTAT" = "YES", and it is this flag that is checked at diamond 90.

If the host 14 had requested as status report, the link 22 proceeds to ST 30, wherein the link 22 transmits the requested status to the host 14 and then clears the "REQSTAT" flag. Then, the link 22 proceeds to ST 5.

In ST 5, "XMITMODE" is set by the MSSTATE 52 to enable the transmit pin of the SED 58. The MSTATE 52 also sends a "transmit SOF" signal to the encoder 70, which causes the encoder 70 to generate signals on the SND0, SND1 lines to cause the SED 58 to generate a pulse on the bus 26 of the appropriate duration for a SOF. A TRPRE signal is asserted at ST 5 to drive the preset input of the flip-flops in the SED 58 to "start" the SED 58.

Also, in ST 5 the status of an EOD flag is latched to a status byte in the RSSTATE 58. The latching of the EOD flag occurs just prior to a blast transfer (disclosed further below) of data between the host 14 and link 22. Additionally, in ST 5 a "blast" flag is set to connect the MISO pin (and, hence, the data buffer of the host 14) with the byte buffer 64, so that the message data in the host 14 can be serially transferred, bit by bit, to the link 22 in a so-called "blast" transfer. The idle pin is reset, as are the CRCGEN 66 and CRCCHECK 68 circuits, i.e., the CRC circuits of the link 22 are initialized at ST 5.

From ST 5 the link 22 proceeds to ST 6, wherein a byte of data is transferred from the host 14, through the CRCGEN 66 and high level logic gates 72 to the byte buffer 64. To effect this transfer, each microsecond the clocking signals to the byte buffer 62 are toggled to transfer one bit from the host 14 into the buffer 64. After each transfer, the MSSTATE 52 determines, at diamond 98, whether all eight bits of the byte being transferred have been transferred, i.e., whether the bit counter = 0. If not, the link 22 loops back to again toggle the clocking signals to transfer another bit, and continues the so-called "blast" transfer - one bit per microsecond - of data from the host 14 into the buffer 64 until all eight bits have been transferred.

As envisioned by the present invention, a blast transfer of data is a data exchange. In other words, when a byte is blast transferred from, e.g., the byte buffer 64 to the host 14, another byte is simultaneously transferred from the host 14 to the byte buffer 64.

Also at ST 6 a byte pin is latched as appropriate to indicate whether the host 14 has indicated that the byte being transferred is the last byte. In the presently preferred embodiment, the host 14 indicates a byte ready by asserting a high voltage on the "byte" input to the STATEIN 54, and the asserted voltage is short unless the byte being transferred is the last byte.

Once the byte has been transferred, the link 22 proceeds to ST 7, wherein the "blast" and "byte ready" flags are cleared. Proceeding to ST 8, the link 22 shifts the last byte flag as appropriate to indicate whether the byte just transmitted was the last byte of the message from the host 14.

The link 22 remains in ST 8 until a high to low bus 26 voltage transition is detected by the SED 58, as indicated by the loop at diamond 100. Such a transition indicates to the link 22 that the SOF symbol transmitted at ST 5 has properly completed transmission on the bus 26.

After reception of the SOF symbol, the link 22 proceeds to ST 10, wherein the next-to-be-transmitted bit (initially, the first bit) of the byte to be transmitted is encoded and transmitted onto the bus 26 by the SED 58. At diamond 102 the link 22 monitors for the proper transmission and return of this bit through the SED 58 by monitoring for a bus 26 voltage transition. If no transition is detected, the MSSTATE 52 determines, at diamond 106, whether an end of data (EOD) symbol has been detected by the SED 58, and if so, proceeds to ST 23. If no EOD symbol is detected at diamond 106, the MSSTATE 52 remains in ST 10.

In contrast, when a bus 26 transition is detected at diamond 102, the MSSTATE 52 determines, at diamond 104, whether the link 22 has won priority to transmit in accordance with the arbitration regime of the particular communications system. If not, the MSSTATE 52 configures the link 22 to ST 11, wherein "XMITMODE" is cleared. From ST 11, or from diamond 104 if the link 22 wins arbitration, the MSSTATE 52 configures the link 22 to ST 12.

In ST 12, data from the bus 26 is transferred into the byte buffer 64 by toggling the clocking signal to the buffer 64. As data is transferred into the buffer 64, the bit counter is incremented. At diamond 108, the MSSTATE 52 determines whether all bits have been encoded and received back off the bus 26. If all bits have not been transmitted, the MSSTATE 52 reconfigures the link 22 to ST 10 to encode and transmit the next subsequent bit.

Otherwise, the MSSTATE 52 determines, at diamond 110, whether the host 14 has asserted a status request. If no status request has been asserted, the link 22 moves to ST 13, wherein the "BLAST" flag is set and the EOD flag is latched. By latching the EOD flag Then, the link moves to ST 14, wherein the data in the byte buffer 64 is blast transferred to the host 14 using the two-way blast technique described above. The data transfer is monitored for completion as indicated by the loop at diamond 112, and upon completion the link 22 moves to ST 15.

If the MSSTATE 52 determines at diamond 110 that a status request has been asserted by the host 14, the link 22 determines, at diamond 114, whether the "XMITMODE" pin is asserted. If it is, the link 22 moves to ST 25 to indicate an error. otherwise, the link 22 moves to ST 31, wherein the link 22 transmits the requested status to the host 14 and waits until the status request has been terminated. Once terminated, the link 22 proceeds to ST 13.

Continuing with the description of Figure 4, at ST 15 the MSSTATE 52 clears the "BLAST" and "OK TO ACK" flags. By consulting the "last byte" flag at diamond 116, the MSSTATE 52 determines whether the byte that has been transmitted is the last data byte to be transmitted onto the

bus 26. If not, the MSSTATE 52 determines at diamond 118 whether the host 14 has signalled a byte ready.

If it is, the link 22 proceeds to ST 17, wherein the last byte flag is shifted to indicate that the last byte of the message from the host 14 has been transmitted and received back by the link 22. Also, the "byte ready" flag is cleared, and the "OK to ack" flag (if the host 14 has indicated that it will transmit an acknowledgement to the message just received) is set. In contrast, if it is determined at diamond 118 that the host 14 has not signalled that a byte is ready, the link proceeds to ST 18, wherein the "byte ready", "last byte", "XMITMODE", and "send CRC" flags are cleared. From either ST 17 or ST 18 the link reconfigures to ST 10.

If it is determined at diamond 116 that the byte that has been transmitted is the last byte, the MSSTATE 52 determines, at diamond 120, whether the EOD flag is set. If not, the MSSTATE 52 determines, at diamond 122, whether the "send CRC flag" is set to indicate that the link 22 has already appended a CRC byte(s) to the message just transmitted. If it is, the MSSTATE 52 reconfigures the link 22 to ST 18. If the "send CRC" flag indicates that a CRC byte has not yet been appended to the message, the MSSTATE 52 proceeds to diamond 124 to determine if the "XMITMODE" flag indicates that transmission is authorized. If not, the link 22 reconfigures to ST 18, but if transmission is authorized, the link 22 proceeds to ST 19.

In ST 19, the MSSTATE 52 sets the "send CRC" flag and causes the generation of a "XMT CRC" signal. The effect of the "XMT CRC" signal is to connect the output of the CRCGEN 66 to the byte buffer 64 for transmission of a CRC message that is generated by the CRCGEN 66 in accordance with the check byte protocol of the particular system 10. At ST 20 the CRC message in the CRCGEN 66 is clocked into the byte buffer 64 by toggling the clock signals in accordance with principles discussed above, with the serial transfer being monitored for completion as indicated by the loop at diamond 126. After transferring the CRC byte into the byte buffer 64, the link 22 reconfigures to ST 21, wherein the "XMT CRC" signal is cleared. From ST 21, the link 22 returns to ST 10 to transmit the CRC byte onto the bus 26 as an appended data string to the host 14 data message previously transmitted.

Recall that the MSSTATE 52 determined at diamond 120 whether an EOD flag was set to indicate the presence of an EOD symbol on the bus 26. If an EOD symbol is detected, the MSSTATE 52 determines at diamond 128 whether an "ACKER" signal has been received by the link 22 pursuant to a host 14-initiated status transfer. Such a signal indicates that the host 14 wants to send an acknowledgement, colloquially referred to as an in-frame response (IFR), as part of the current message frame.

If no "ACKER" signal has been received, the link 22 reconfigures to ST 22. In ST 22, flags representing "ACKER", "NOT MACKER" (otherwise indicating that an IFR is not to be a type 3

IFR), "byte ready", "last byte", "XMITMODE", and "send CRC" are cleared. From ST 22, the link 22 reconfigures to ST 10.

If an "ACKER" signal has been received at diamond 128, the MSSTATE 52 determines at diamond 130 whether transmission is authorized. If so, the MSSTATE 52 determines at diamond 132 whether a CRC message has been appended to the current message frame. If so, the MSSTATE 52 reconfigures the link 22 to ST 22. Otherwise, the MSSTATE 52 moves to diamond 134 to determine whether the "NOT MACKER" flag is set. If the "NOT MACKER" flag indicates that a type 3 IFR has been sent, the link 22 reconfigures to ST 19. Otherwise, the link 22 reconfigures to ST 22.

On the other hand, if it is determined at diamond 130 that transmission is not authorized, the MSSTATE 52 next determines, at diamond 136, whether the "NOT MACKER" flag is set. If it is not, the link 22 moves to ST 22. If the "NOT MACKER" flag is set, the MSSTATE 52 determines at diamond 138 whether an acknowledgement byte is ready. If not, the link 22 moves to ST 22, but if it is, the link 22 moves to ST 16. At ST 16, the "XMITMODE" flag is set and the "byte ready" flag is reset. The link then returns to ST 10 to transmit an IFR byte.

Recall that the link 22 enters ST 23 when an EOD condition is detected on the bus 26 at diamond 106 (which event happens after the last byte has been transmitted). ST 23 and related operations are used for appending check bytes (CRC messages) to the main message from the host 14, after an EOD condition is detected subsequent to transmitting the main message.

At ST 23, "XMITMODE" is cleared and the EOD flag is set to indicate the presence of an EOD symbol on the bus 26. Also, "CRC OK" flag is latched. By so latching this last signal, the output of the CRCCHECK 68, which indicates whether the received data is good or bad, can be communicated through the RSSTATE 60 to the host 14 when the host 14 initiates a status request via the REQSTAT input pin.

At diamond 140 the MSSTATE 52 determines, based on the output of the CRCCHECK 68, whether the received message was OK. If not, the link 22 resets to ST 1. If the received message was OK, the MSSTATE 52 determines whether the bit counter = 0 at diamond 142. If not, the link 22 reconfigures to ST 25 to indicate an error, but if the bit counter = 0, the MSSTATE 52 moves to diamond 144 to determine if the "ACKER" flag is set.

If the "ACKER" flag is set, the MSSTATE 52 moves to diamond 146 to determine whether the "OK to ack" flag is set, and if it isn't, the link 22 reconfigures to ST 25 to indicate an error. In accordance with the present invention, the "OK to ack" feature prevents the host 14 from erroneously transmitting an acknowledgement (referred to as an in-frame response, or IFR) to a degraded message. Without the logic disclosed below, such an event could occur after receipt of a first "good byte" (which informs the host 14 whether an IFR should be transmitted), followed by degraded subsequent bytes combined with a failure of the CRCCHECK 68 to properly indicate such degradation.

If the "OK to ack" flag is set, the link 22 moves to ST 26, wherein the "XMITMODE" flag is set and an EOD symbol is transmitted, which, as can be recalled in reference to Figure 2, occurs before an acknowledging IFR is appended to a message. Diamond 148 is a loop test that sends the MSSTATE 52 to diamond 150 once a high voltage on the bus 26 is detected.

At diamond 150, the MSSTATE 52 determines, based on the "NOT MACKER" flag, whether the host 14 has indicated a type 3 IFR is to be appended to the message. If so, the MSSTATE 52 configures the link 22 to ST 27 to transmit a long normalization bit, indicating that a type 3 IFR is to follow. Otherwise, the MSSTATE 52 configures the link 22 to ST 28 to disable the latch "CRC OK" and to transmit a short normalization bit, indicating that a type 1 or type 2 IFR is to follow.

From ST 27, the MSSTATE 52 determines, at diamond 154, whether a high to low bus 26 voltage transition occurs (indicating that the long normalization bit has been properly transmitted and returned). If not, the link 22 remains in ST 27. Once the normalization bit is detected on the bus 26, the link 22 reconfigures to ST 9 to process the IFR from the host 14 in accordance with principles discussed above. Likewise, from ST 28, the MSSTATE 52 determines, at diamond 152, whether a high to low bus 26 voltage transition occurs (indicating that the normalization bit has been properly transmitted and returned). If not, the link 22 remains in ST 28. Once the normalization bit is detected on the bus 26, the link 22 reconfigures to ST 9 to process the IFR from the host 14 in accordance with principles discussed above.

Recall that at diamond 144 the MSSTATE 52 determined whether the "ACKER" flag was set. If it wasn't, the MSSTATE 52 configures the link 22 to ST 24, wherein the "NOT MACKER" and "ACKER" flags are cleared. Then, at diamond 156, the MSSTATE 52 determines whether a high to low bus 26 voltage transition occurs (indicating reception of a normalization bit). If not, the MSSTATE 52 determines at diamond 158 whether an EOF symbol is present on the bus 26, and if not, remains in ST 24 to resume the diamond 156 test. On the other hand, if an EOF symbol is detected, the link 22 resets to ST 2.

If it is determined at diamond 156 that a high to low bus 26 voltage transition occurs, indicating the start of another node's IFR transmission, the MSSTATE 52 configures the link 22 to ST 29, wherein the CRC OK latch is disabled if the normalization bit was a short bit. Then, the link resets to ST 9 to receive the IFR.

While the particular VEHICLE COMMUNICATIONS BUS LINK WITH STATE MACHINE as herein shown and described in detail is fully capable of attaining the above-described objects of the invention, it is to be understood that it is the presently preferred embodiment of the present invention and is thus representative of the subject matter which is broadly contemplated by the present invention, that the scope of the present invention fully encompasses other embodiments which may become

obvious to those skilled in the art, and that the scope of the present invention is accordingly to be limited by nothing other than the appended claims.

WHAT IS CLAIMED IS:

1. A communications link for transmitting data between a host microprocessor (host) in a vehicle and a communications bus, comprising:

a signal encoder/decoder (SED) electrically connected to the bus for converting bus signals from the bus to corresponding link signals and for converting link signals to corresponding bus signals;

a byte buffer electrically connected to the host for solicited reception of a first byte of data of a first message from the host when the host generates a byte ready signal, and for unsolicited serial reception of subsequent bytes of the first message thereafter; and

a state machine electrically connected to the byte buffer and SED and embodying logic for establishing data transmission therebetween, the state machine causing the SED to transmit to the bus a data message including the bytes of the first message, the state machine further causing the generation of a start of frame (SOF) symbol only when either: the communications bus is idle, or a predetermined voltage occurs on the communications bus within a predetermined period.

2. The communications link of Claim 1, wherein the state machine further causes the appending of end of data (EOD) symbols and end of frame (EOF) symbols to the data message.

3. The communications link of Claim 2, further comprising a status/control circuit (RSSTATE) electrically connected to the state machine and host for transmitting status bytes to the host in response to a status signal therefrom and for receiving control bytes from the host.

4. The communications link of Claim 3, wherein the state machine appends an in-frame response to the data message in response to a predetermined control signal received from the host by the RSSTATE.

5. The communications link of Claim 4, wherein the state machine includes a bit counter for counting bits during data transmission and reception.

6. The communications link of Claim 5, wherein the state machine causes an SOF symbol to be transmitted in response to a byte ready signal from the host.

7. The communications link of Claim 6, wherein the state machine causes a byte received from the SED and stored in the byte buffer to be transmitted to the host without solicitation from the host.

8. The communications link of Claim 7, wherein the state machine causes a byte after the first byte of the first message to be received unsolicited into the byte buffer after the immediately preceding byte has been transmitted.

9. The communications link of Claim 8, wherein the state machine appends a CRC symbol to the data message when no CRC symbol has previously been appended to the message.

10. The communications link of Claim 9, wherein the host is a first host, and the predetermined transition and predetermined period are representative of the presence of an SOF signal from a host other than the first host.

11. A vehicle, comprising:

a communications bus;

a plurality of component host microprocessors (hosts), each host being electrically connected to the communications bus via a respective link, each link being characterized by logic circuitry for performing method steps to transmit and receive messages between the hosts via the communications bus, each link comprising:

a signal encoder/decoder (SED) electrically connected to the bus for converting bus signals from the bus to corresponding link signals and for converting link signals to corresponding bus signals;

a byte buffer electrically connected to the respective host for solicited reception of a first byte of data of a first message from the host when the host generates a byte ready signal, and for unsolicited serial reception of subsequent bytes of the first message thereafter; and

a state machine electrically connected to the byte buffer and SED and embodying logic for establishing data transmission therebetween, the state machine causing the SED to transmit to the bus a data message including the bytes of the first message, the state machine further causing the generation of a start of frame (SOF) symbol only when either: the communications bus is idle, or a predetermined voltage occurs on the communications bus within a predetermined period.

12. The vehicle of Claim 11, wherein each state machine further causes the appending of end of data (EOD) symbols and end of frame (EOF) symbols to the data message.

13. The vehicle of Claim 12, wherein each link further comprises a status/control circuit (RSSTATE) electrically connected to the respective state machine and respective host for transmitting status bytes to the host in response to a status signal therefrom and for receiving control bytes from the host.

14. The vehicle of Claim 13, wherein each state machine appends an in-frame response to the respective data message in response to a predetermined control signal received from the respective host by the respective RSSTATE.

15. The vehicle of Claim 14, wherein each state machine includes a bit counter for counting bits during data transmission and reception.

16. The vehicle of Claim 15, wherein each state machine causes an SOF symbol to be transmitted in response to a byte ready signal from the respective host.

17. The vehicle of Claim 16, wherein each state machine causes a byte received from the respective SED and stored in the respective byte buffer to be transmitted to the respective host without solicitation from the host.

18. The vehicle of Claim 17, wherein each state machine causes a byte after the first byte of the first message to be received unsolicited into the byte buffer after the immediately preceding byte has been transmitted.

19. The vehicle of Claim 18, wherein the state machine appends a CRC symbol to the data message when no CRC symbol has previously been appended to the message.

20. The vehicle of Claim 19, wherein the predetermined transition and predetermined period are representative of the presence of an SOF signal from a host other than the respective host.

21. A state machine link for interconnecting a host microprocessor (host) in a vehicle to a communications bus in the vehicle, comprising:

buffer means for receiving a first byte of a first message from the host in response to a solicitation signal from the host;

means for causing bytes of the first message subsequent to the first byte to be serially received into the buffer means; and

means for transmitting a start of frame (SOF) symbol onto the bus in response to the solicitation signal only when: the bus is idle, or a voltage transition is present on the bus.

22. The state machine link of Claim 21, further comprising means for appending end of data (EOD) symbols and end of frame (EOF) symbols to the message.

23. The state machine link of Claim 21, further comprising means for transmitting status bytes to the host in response to a status signal therefrom and for receiving control bytes from the host.

24. The state machine link of Claim 21, further comprising means for appending an in-frame response to the message in response to a predetermined control signal received from the host.

25. The state machine link of Claim 21, further comprising means for counting bits during data transmission and reception.

26. The state machine link of Claim 21, further comprising means for transmitting an SOF symbol in response to a byte ready signal from the host.

27. The state machine link of Claim 21, further comprising means for causing a byte to be transmitted to the host without solicitation from the host.

28. The state machine link of Claim 21, further comprising means for unsolicited transfer from the host of a byte after the first byte of the first message.

29. The state machine link of Claim 21, further comprising means for appending a CRC symbol to the message when no CRC symbol has previously been appended to the message.

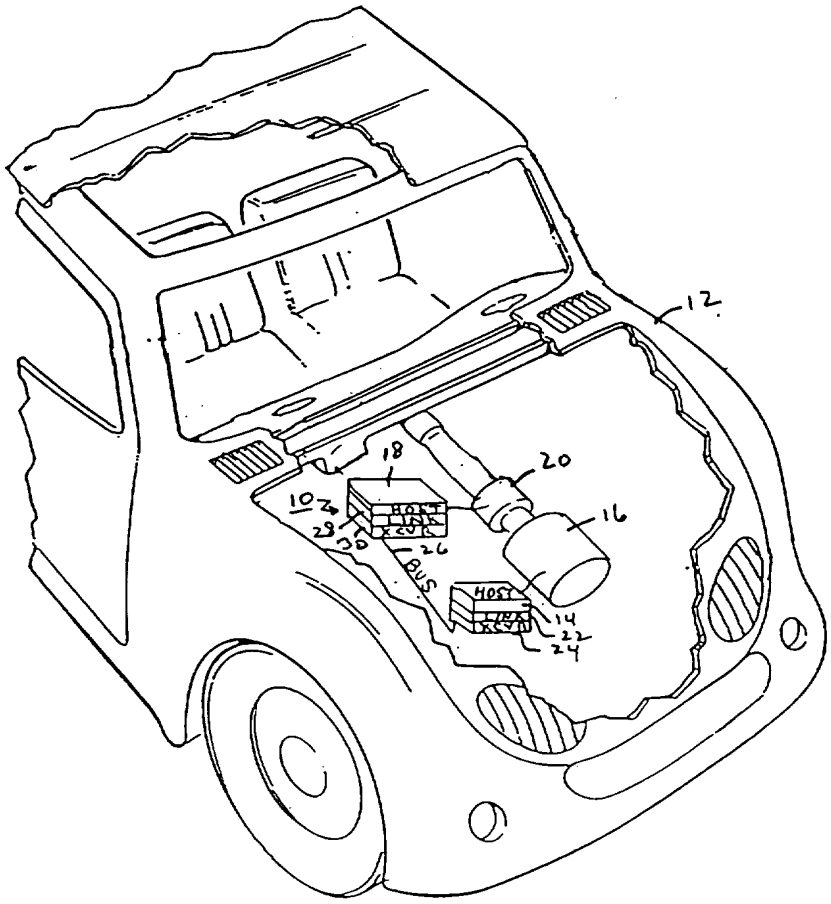
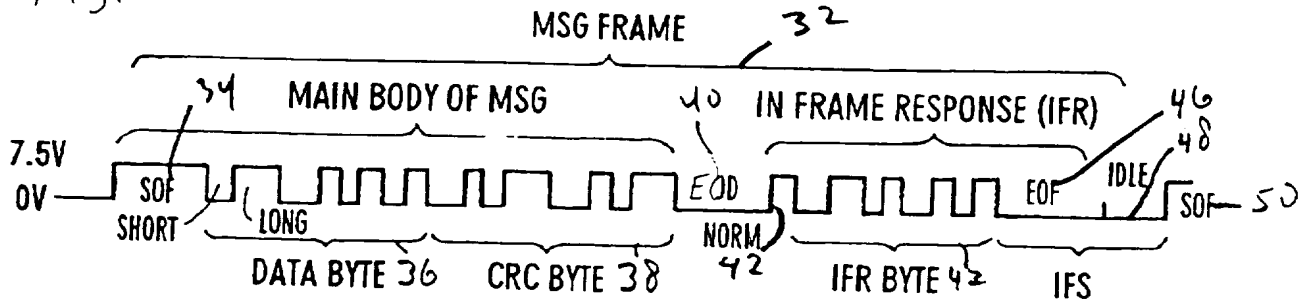


FIGURE 1

Fig. 2



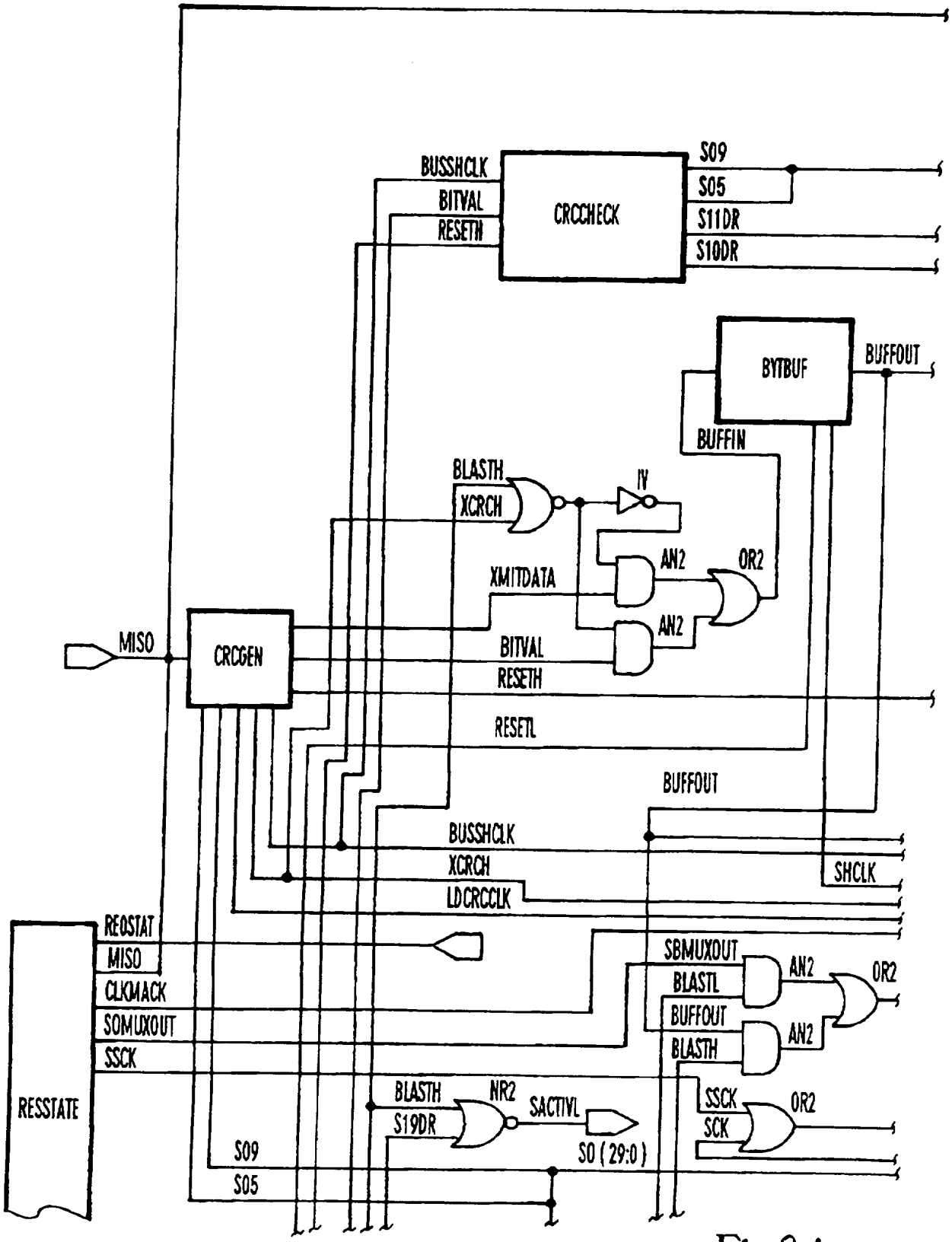

BUSSHCLK
BITVAL
RESETH
CRCCHECK
S09
S05
S11DR
S10DR
BYTBUF
BUFFOUT
BUFFIN
BLASTH
XCRCH
IV
AN2
OR2
XMITDATA
AN2
MISO
CRCGEN
BITVAL
RESETH
RESETL
BUFFOUT
BUSSHCLK
XCRCH
LDCRCCLK
SHCLK
REQSTAT
MISO
CLKMACK
SDMUXOUT
SSCK
SBMUXOUT
BLASTL
AN2
OR2
BUFFOUT
BLASTH
AN2
RESSTATE
BLASTH
S19DR
NR2
SACTIVL
S0 (29:0)
SSCK
SCK
OR2
S09
S05

Fig.3A

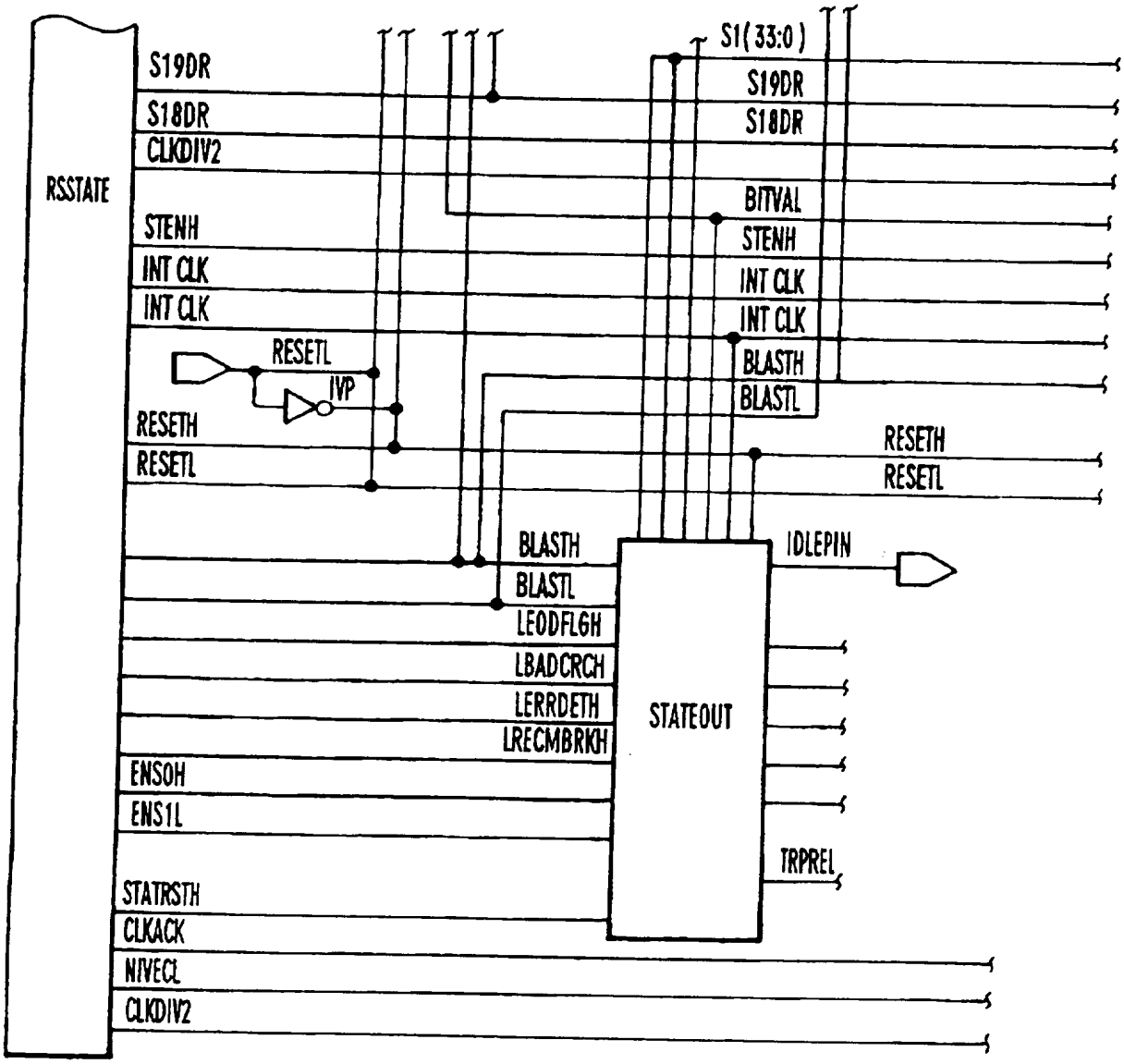

RSSTATE
S19DR
S18DR
CLKDIV2
STENH
INT CLK
INT CLK
RESETL
IVP
RESETH
RESETL
BLASTH
BLASTL
LEODFLGH
LBADCRCH
LERRDETH
LRECMBRKH
ENSOH
ENS1L
STATRSTH
CLKACK
NIVECL
CLKDIV2
S1(33:0)
S19DR
S18DR
BITVAL
STENH
INT CLK
INT CLK
BLASTH
BLASTL
RESETH
RESETL
IDLEPIN
STATEOUT
TRPREL

Fig.3B

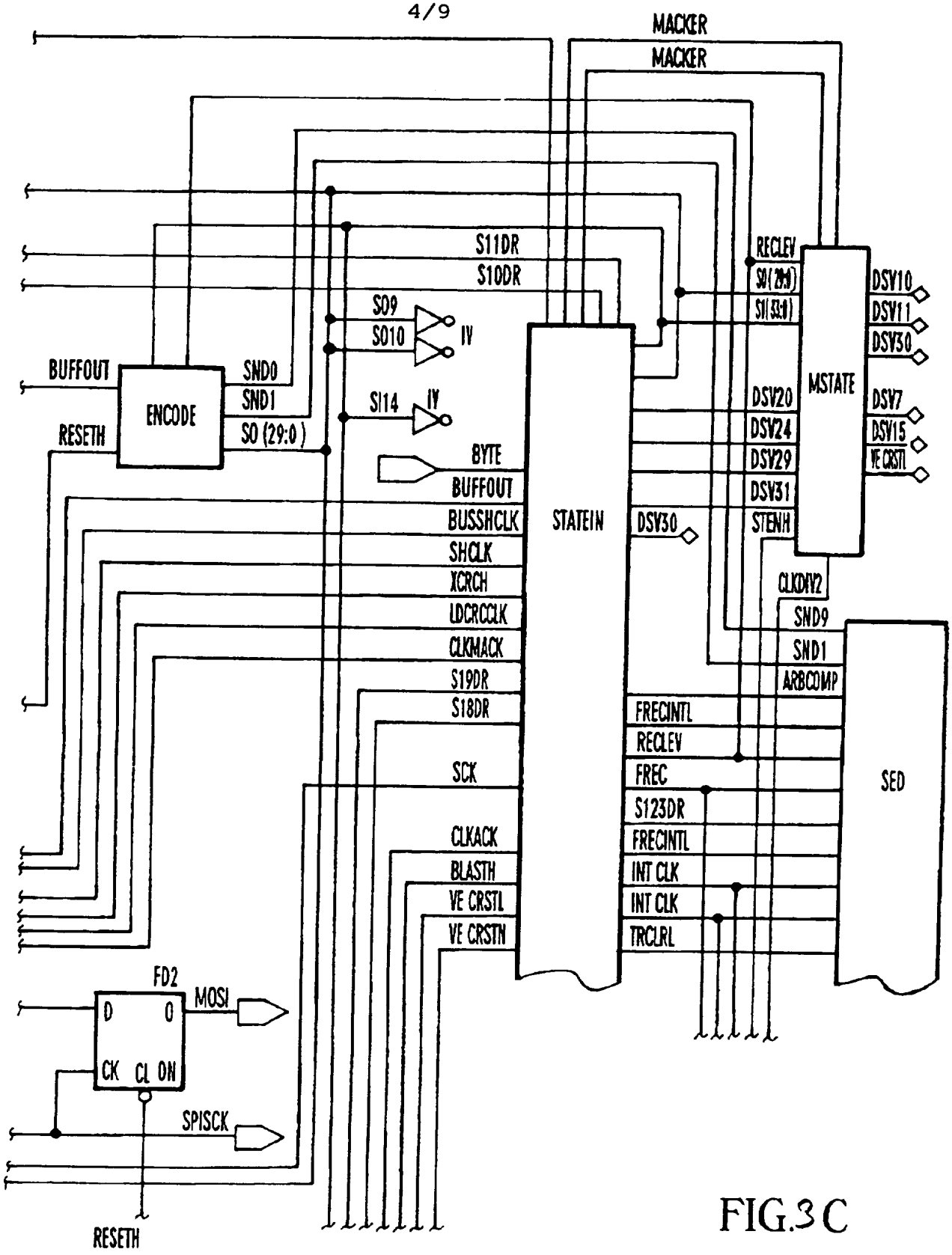

MACKER
MACKER
S11DR
S10DR
S09
S010
IV
BUFFOUT
ENCODE
SND0
SND1
S0 (29:0)
RESETH
S114
IV
BYTE
BUFFOUT
BUSSHCLK
SHCLK
XCRCH
LDCRCCLK
CLKMACK
S19DR
S18DR
SCK
CLKACK
BLASTH
VE CRSTL
VE CRSTN
STATEIN
DSV30
RECLEV
S0(29:0)
S1(53:0)
DSV20
DSV24
DSV29
DSV31
STENH
MSTATE
DSV10
DSV11
DSV30
DSV7
DSV15
VE CRSTL
CLKDIV2
SND9
SND1
ARBCOMP
FRECINTL
RECLEV
FREC
S123DR
FRECINTL
INT CLK
INT CLK
TRCLRL
SED
FD2
D
Q
CK
CL
ON
MOSI
SPISCK
RESETH

FIG.3C

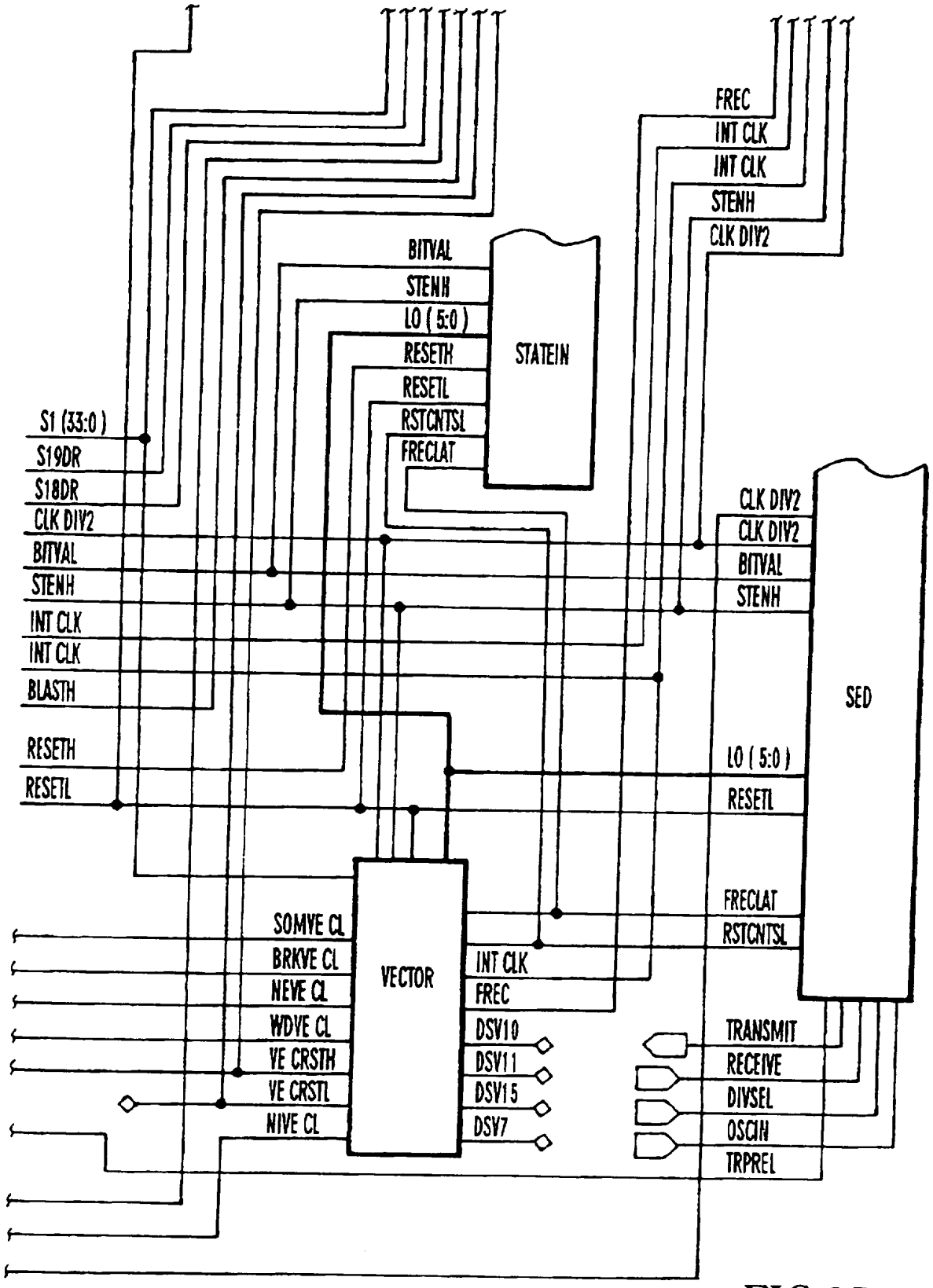

FREC
INT CLK
INT CLK
STENH
CLK DIV2
BITVAL
STENH
LO (5:0)
RESETH
RESETL
RSTCNTSL
FRECLAT
STATEIN
S1 (33:0)
S19DR
S18DR
CLK DIV2
BITVAL
STENH
INT CLK
INT CLK
BLASTH
RESETH
RESETL
CLK DIV2
CLK DIV2
BITVAL
STENH
LO (5:0)
RESETL
FRECLAT
RSTCNTSL
SED
SOMVE CL
BRKVE CL
NEVE CL
WDVE CL
VE CRSTH
VE CRSTL
NIVE CL
VECTOR
INT CLK
FREC
DSV10
DSV11
DSV15
DSV7
TRANSMIT
RECEIVE
DIVSEL
OSCIN
TRPREL

FIG.3 D

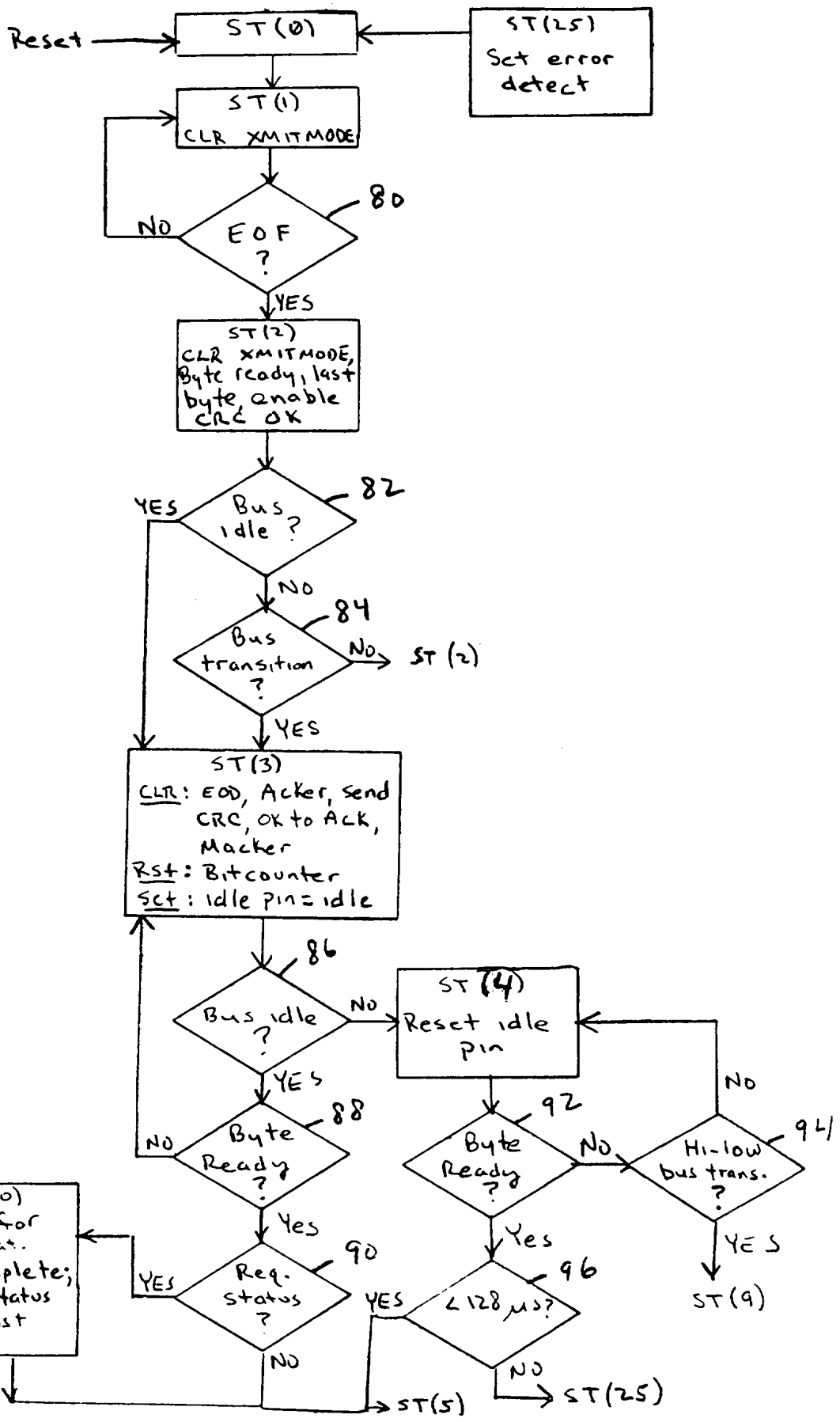

Reset
ST(0)
ST(25)
Set error detect
ST(1)
CLR XMITMODE
80
NO
EOF ?
YES
ST(2)
CLR XMITMODE, Byte ready, last byte, enable CRC OK
82
YES
Bus idle ?
NO
84
Bus transition ?
NO
ST(2)
YES
ST(3)
CLR: EOD, Acker, Send CRC, OK to Ack, Macker
Rst: Bitcounter
Set: idle pin = idle
86
Bus idle ?
NO
ST(4)
Reset idle pin
YES
88
Byte Ready ?
NO
YES
92
Byte Ready ?
NO
94
Hi-low bus trans. ?
NO
YES
ST(9)
ST(30)
Wait for req. stat. to complete; Xmit status to host
90
Req. status ?
YES
NO
Yes
96
< 128 μs?
YES
NO
ST(25)
ST(5)

Fig. 4A

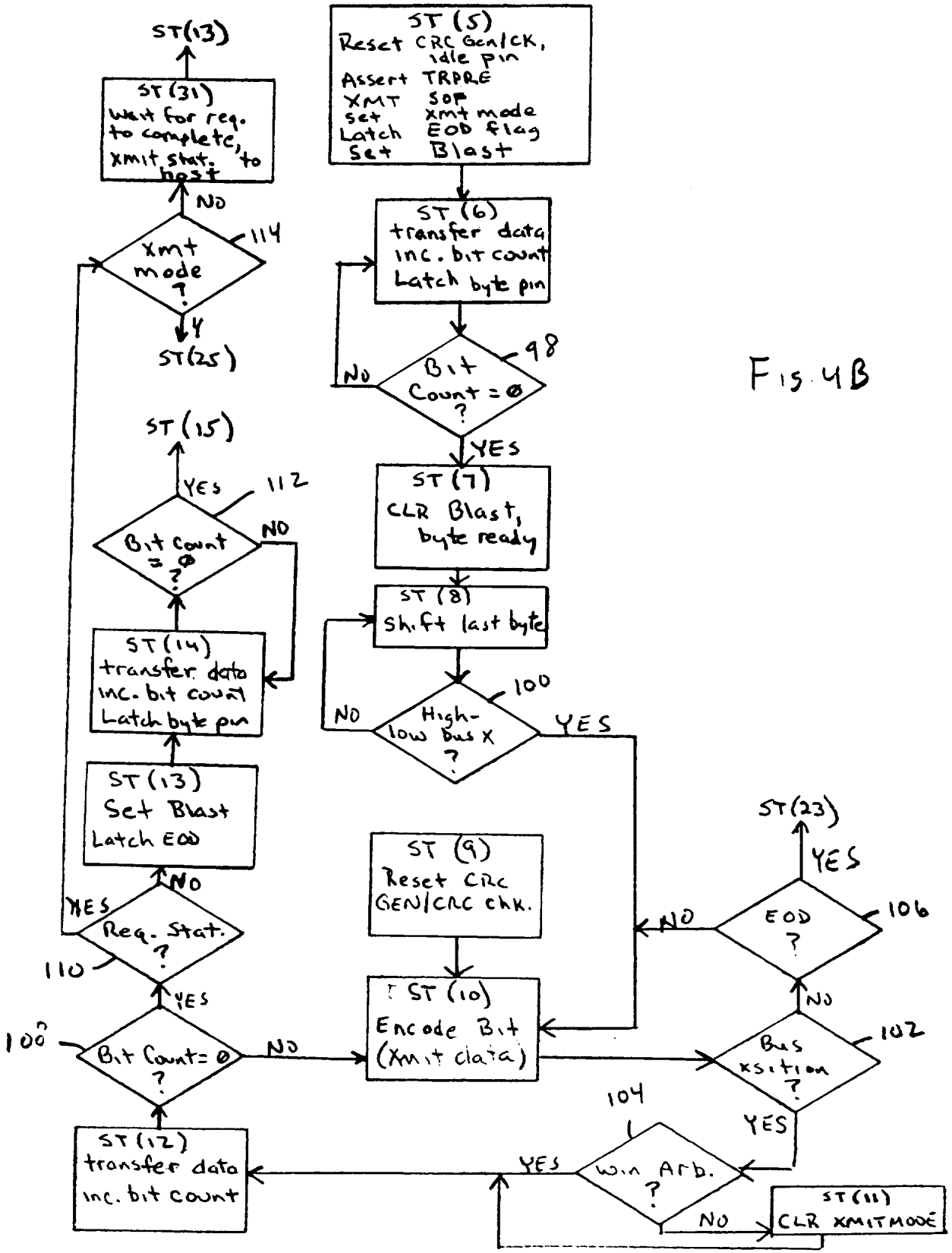

ST (5)
Reset CRC Gen/CK, idle pin
Assert TRPRE
XMT SOP set xmt mode
Latch EOD flag
Set Blast
ST (6)
transfer data inc. bit count
Latch byte pin
Bit Count = 0 ?
98
NO
YES
ST (7)
CLR Blast, byte ready
ST (8)
Shift last byte
High-low Bus X ?
100
NO
YES
ST (9)
Reset CRC GEN/CRC chk.
ST (10)
Encode Bit (Xmit data)
Bus xsition ?
102
NO
YES
EOD ?
106
NO
YES
ST(23)
Win Arb. ?
104
YES
NO
ST (11)
CLR XMITMODE
ST (12)
transfer data inc. bit count
Bit Count = 0 ?
100
NO
YES
Req. Stat. ?
110
NO
YES
ST (13)
Set Blast
Latch EOD
ST (14)
transfer data inc. bit count
Latch byte pin
Bit count = 0 ?
112
NO
YES
ST (15)
Xmt mode ?
114
NO
Y
ST(25)
ST (31)
Wait for req. to complete, xmit stat. to host
ST(13)

Fig. 4B

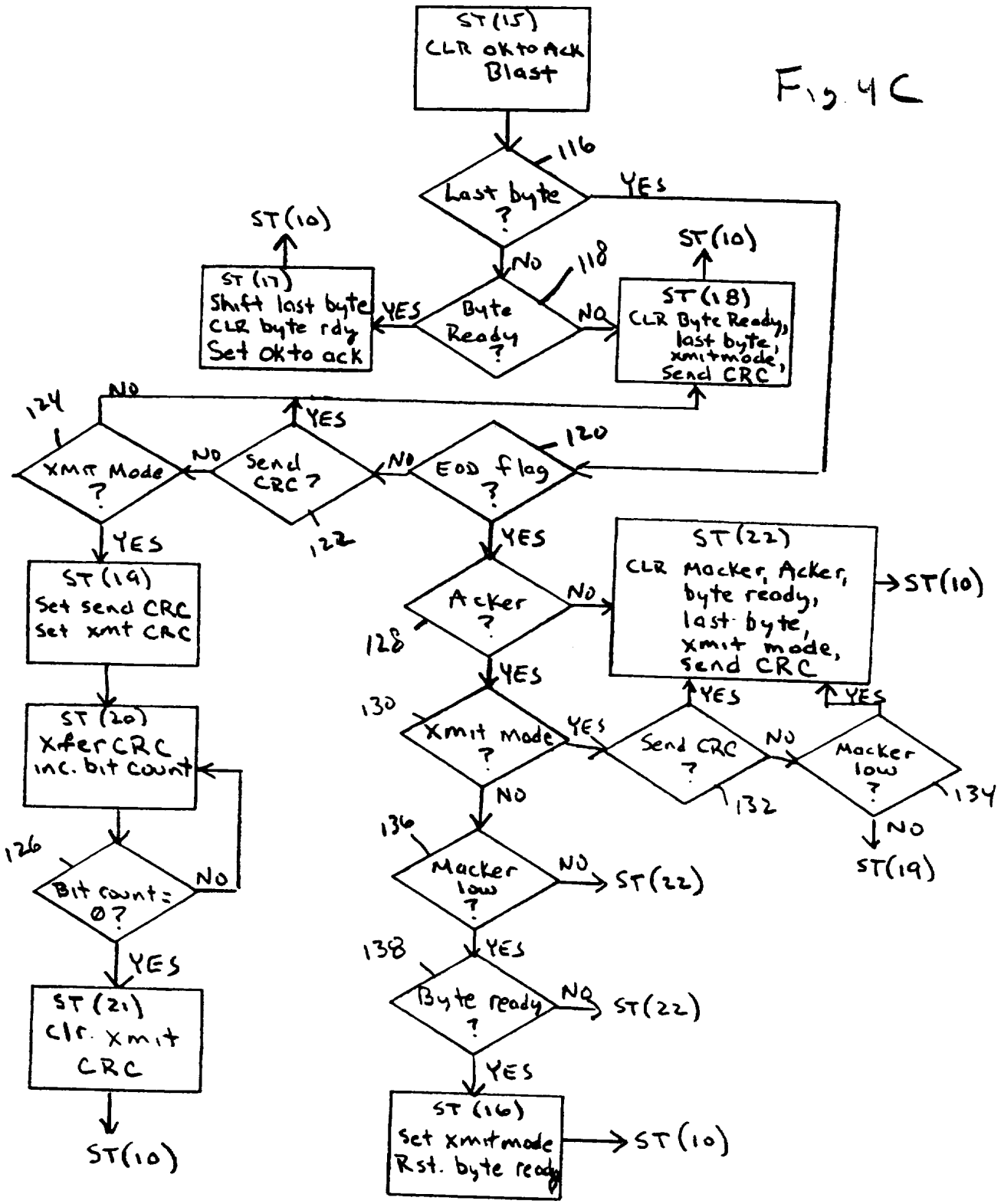

ST(15)
CLR ok to Ack
Blast
116
Last byte ?
YES
NO
ST(10)
ST(17)
Shift last byte
CLR byte rdy
Set ok to ack
118
Byte Ready ?
YES
NO
ST(10)
ST(18)
CLR Byte Ready,
last byte,
xmit mode,
Send CRC
124
NO
YES
Xmit Mode ?
NO
Send CRC ?
NO
EOD flag ?
120
122
YES
YES
ST(19)
Set send CRC
Set xmt CRC
ST(20)
XferCRC
inc. bit count
126
Bit count = 0 ?
NO
YES
ST(21)
Clr. xmit CRC
ST(10)
ST(22)
CLR Macker, Acker,
byte ready,
last byte,
xmit mode,
Send CRC
ST(10)
Acker ?
NO
128
YES
130
Xmit mode ?
YES
Send CRC ?
NO
YES
YES
132
Macker low ?
134
NO
ST(19)
NO
136
Macker low ?
NO
ST(22)
YES
138
Byte ready ?
NO
ST(22)
YES
ST(16)
Set xmit mode
Rst. byte ready
ST(10)

Fig. 4C

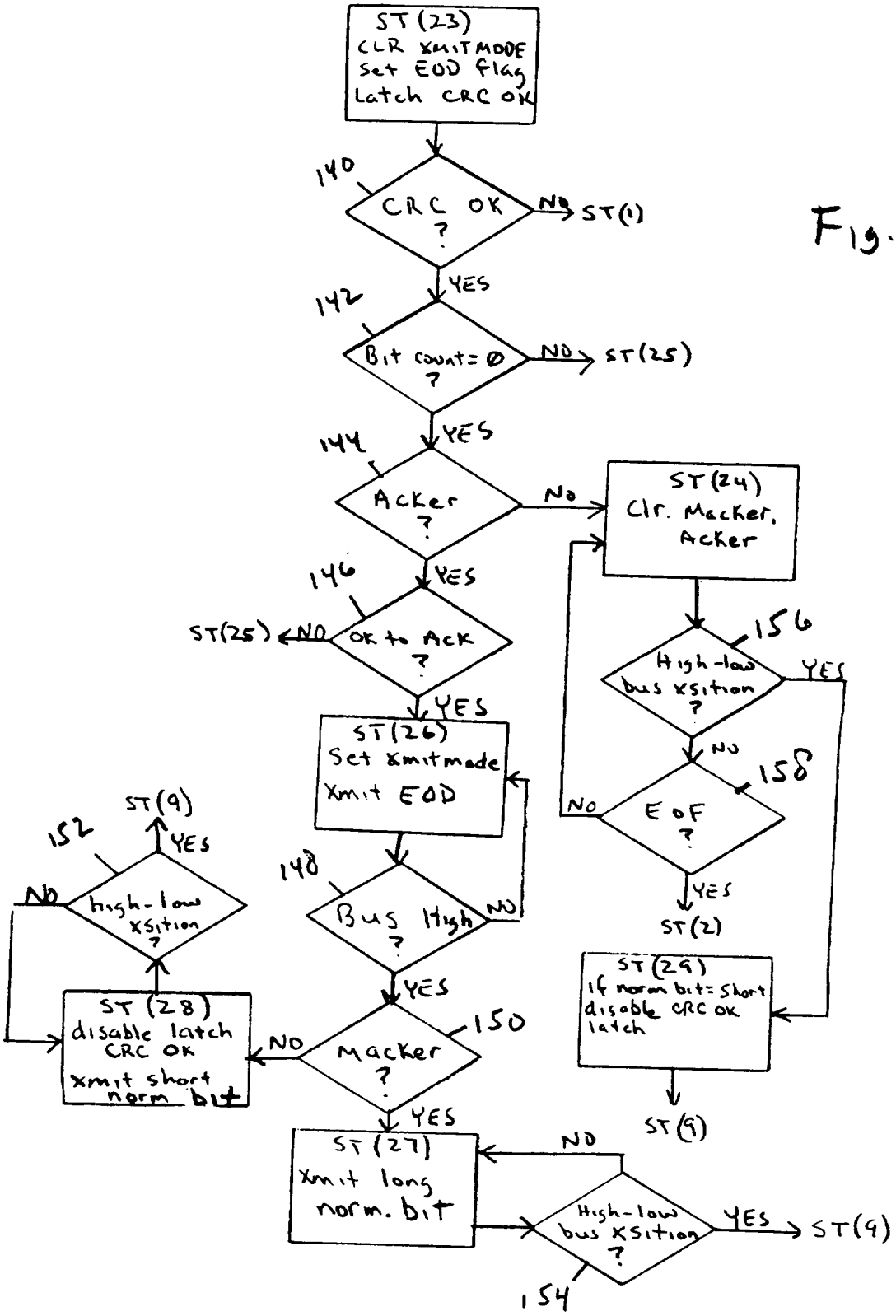

ST (23)
CLR XmitMode
Set EOD flag
Latch CRC OK
140
CRC OK ?
NO
ST(1)
YES
142
Bit count = 0 ?
NO
ST(25)
YES
144
Acker ?
No
ST(24)
Clr. Macker, Acker
YES
146
ST(25)
NO
OK to Ack ?
YES
ST(26)
Set xmitmode
Xmit EOD
156
High-low bus xsition ?
YES
NO
158
No
EOF ?
YES
ST(2)
ST(29)
If norm bit = short
disable CRC OK latch
ST(9)
148
Bus High ?
NO
YES
ST(9)
152
YES
No
high-low xsition ?
ST (28)
disable latch
CRC OK
xmit short norm bit
NO
150
Macker ?
YES
ST (27)
Xmit long norm. bit
NO
High-low bus xsition ?
YES
ST(9)
154

Fig. 4D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/16470

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H04J 3/02

US CL :370/9, 85.1, 85.2, 85.3, 99; 340/825.06, 825.07, 825.5

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/9, 85.1, 85.2, 85.3, 99; 340/825.06, 825.07, 825.5

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 5,274,636 (HALTER ET AL) 28 December 1993, see entire reference.	1-29
A	US, A, 5,287,523 (ALLISON ET AL) 15 February 1994, column 3, lines 51-57.	1-29
A,P	US, A, 5,402,420 (KOBAYASHI) 28 March 1995, see entire reference.	1-29

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be part of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

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Date of the actual completion of the international search	Date of mailing of the international search report
11 MARCH 1996	21 MAR 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer MELVIN MARCELO Telephone No. (703) 305-4700

Form PCT/ISA/210 (second sheet)(July 1992)★